CLAIMS

WHAT IS CLAIMED IS:

1. A method of fabricating a capacitor over a first layer having a first conductive plug formed on a substrate in a semiconductor memory, the capacitor fabrication method comprising the steps of:

forming a silicon nitride film on the first layer;

forming a first capacitor oxide film on the silicon nitride film;

forming a second capacitor oxide film over the first capacitor oxide film, wherein the wet etch rate of the first capacitor oxide film is different from the etch rate of the second capacitor oxide film;

performing etching to a selected portion of the first and second capacitor oxide films using the silicon nitride film as an etch stopper to form at least one second contact hole for a storage node electrode, wherein the second contact hole is etched until the first conductive plug of the first layer is exposed;

sequentially forming a silicon film for storage node electrode and a filler film on the resultant surface of the first and second capacitor oxides including the surface of the second contact hole;

forming a cylindrical storage node electrode by etching a predetermined portion of the filler film and the silicon film until the surfaces of the first and second capacitor oxide films are exposed to form a cylindrical storage node electrode;

sequentially removing the remaining filler film and first and second oxide films; and

sequentially forming a Ta_2O_5 dielectric film covering the storage node electrode and a TiN film for an upper electrode.

2. The method as set forth in claim 1, wherein the silicon nitride film is formed at a thickness of 200 to 1000Å by using Low Pressure Chemical Vapor Deposition (LP-CVD) or Plasma Enhanced Chemical Vapor Deposition (PECVD).

3. The method as set forth in claim 1, wherein the etching of the first and second capacitor oxide film is sequentially performed dry etching and wet etching.

4. The method as set forth in claim 1, wherein the first capacitor oxide film is any one of a Phospho-Silicate-Glass (PSG), Boro-Phosphor-Silicate Glass (BPSG), Low Pressure Tetra-Ethyl-Ortho-Silicate (LP-TEOS), and a second capacitor

oxide film is made of Plasma Enhanced Tetra-Ethyl-Ortho-Silicate (PE-TEOS).

5. The method as set forth in claim 4, wherein the first capacitor oxide film has a wet etch rate that causes the first capacitor oxide film to be etched faster than the second capacitor oxide film.

6. The method as set forth in claim 1, wherein the dry etching of the first and second capacitor oxide films is performed to an over-etch target for 10 to 100%.

7. The method as set forth in claim 1, wherein etch selectivity of the first and second capacitor oxide films to the silicon nitride film is maintained in a range of 5:1 to 20:1.

8. The method as set forth in claim 3, wherein the wet etching of the first and second capacitor oxide films makes use of any one of an HF solution to which H_2O_2 and ultra pure water are added and an HF/NH4F mixture solution to which H_2O_2 and ultra pure water are added, as a wet etch solution.

9. The method as set forth in claim 1, wherein the silicon film for a storage node electrode is formed at thickness of 200 to 600Å.

10. The method as set forth in claim 1 or 9, wherein the step of forming the silicon film for the storage node electrode comprises the steps of:

depositing a polycrystalline silicon film doped with dopants to a first thickness on the resulting surface of the second capacitor oxide film including the surface inside the second contact hole for forming a storage node electrode, wherein the first thickness is from 30 to 70 % of the thickness of the storage node electrode;

depositing a silicon film, which is not doped with amorphous dopants, to a second thickness on the polycrystalline silicon film doped with dopants, wherein sum of the first thickness and the second thickness is the thickness of the storage node electrode; and

performing heat treatment to the resultant structure to grow Hemi-Spherical Gains (HSGs) to a radius of 50 to 300 Å.

11. The method as set forth in claim 1, wherein the step of etching the silicon film for a storage node electrode is performed to the over-etch target for 5 to 10 %.

12. The method as set forth in claim 1, wherein the filler film is any one of a photosensitive film and Undoped Silicate Glass (USG) film.

13. The method as set forth in claim 1, further comprising a step of performing thermal doping treatment under an atmosphere of phosphorus containing gas after the step of forming the silicon film for the storage node electrode.

14. The method as set forth in claim 13, wherein the step of thermal doping treatment is performed in a furnace at a temperature of 600 to 700 ℃ under a pressure of 1 to 100 torr for 30 to 120 minutes.

15. The method as set forth in claim 13, further comprising a step of performing Rapid Thermal Process (RTP) to the substrate including the silicon film for a storage node electrode at a temperature of 700 to 950℃ for 10 to 100 seconds, prior to the step of thermal doping treatment.

16. The method as set forth in claim 1, further comprising the steps of:

performing primary heat treatment after forming the Ta_2O_5 dielectric film to remove carbon impurities and oxygen vacancies in the Ta_2O_5 dielectric film; and

performing secondary heat treatment in situ after forming the TiN film for the upper electrode on the surface of the resulting structure to remove Cl ions from the TiN film.

17. The method as set forth in claim 1, further comprising: prior to forming the Ta_2O_5 dielectric film, performing nitrification in a furnace or using plasma at a temperature of 400 to 700 ℃ under an NH_3 atmosphere.

18. The method as set forth in claim 16, wherein the primary heat treatment is performed at the temperature of 600 to 800 ℃ under the atmosphere of N_2O or O_2.

19. The method as set forth in claim 16, further comprising: before or after performing the primary heat treatment, performing RTP under an atmosphere of O_2 and N_2.

20. The method as set forth in claim 1, wherein the step of

forming a TiN film for an upper electrode comprises the steps of:

forming a first TiN film by CVD; and

forming a second TiN film on the first TiN film via sputtering.